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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,695	08/20/2003	Atousa Soroushi	VP075	6704
20178	7590	06/16/2008	EXAMINER	
EPSON RESEARCH AND DEVELOPMENT INC INTELLECTUAL PROPERTY DEPT 2580 ORCHARD PARKWAY, SUITE 225 SAN JOSE, CA 95131				ELMORE, REBA I
ART UNIT		PAPER NUMBER		
2189				
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			06/16/2008	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/644,695	SOROUSHI, ATOUSA	
	<b>Examiner</b>	<b>Art Unit</b>	
	Reba I. Elmore	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 01 April 2008.  
 2a) This action is **FINAL**.                            2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-3, 12, 13, 23-25, 37 and 38 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-3, 12-13, 23-25 and 37-38 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____.	6) <input type="checkbox"/> Other: _____ .

## **DETAILED ACTION**

1. Claims 1-3, 12-13, 23-25 and 37-38 are presented for examination. Claims 4-11, 14-22, 26-36 and 39-50 have been cancelled.

### ***SPECIFICATION***

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### ***35 USC § 112, 1<sup>st</sup> Paragraph***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 3 is incomplete, steps (c)-(f) are missing from the claim.

### ***35 USC § 102***

6. The rejection of claims 1-3, 12-13, 23-25 and 37-38 as being anticipated by Wollan et al. is **maintained** and repeated below with changes to include the amendments to the claims.

7. The following is a quotation of the appropriate paragraphs of 35 USC 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-3, 12-13, 23-25 and 37-38 are rejected under 35 USC 102(b) as being anticipated by Wollan et al. (P/N 5,809,327).
9. Wollan teaches the invention (claim 1) as claimed including a method for accessing a device by a host using a dedicated bus, the device having up to  $2^M$  memory locations, the bus having N data lines and at least two control lines, wherein M is greater than N, and the host performs an address cycle by asserting a first control signal and a data cycle, the present claimed invention comprising:
  - (a) performing a first address cycle to transmit a first address portion over the bus during the first address cycle;
  - (b) storing the first address portion in a first register of the device in response to detecting the first address cycle; steps (a) and (b) are taught as transmitting and storing the first half of a sixteen bit address (e.g., see col. 4, lines 20-28);
  - (c) performing a second address cycle to transmit a second address portion over the bus during the second address cycle;
  - (d) storing the second address portion in a second register of the device in response to detecting the second address cycle; steps (c) and (d) are taught as transmitting and storing the second half of the sixteen bit address (e.g., see col. 4, lines 20-28);
  - (e) performing a first data cycle if the first and second address portions, when combined, form a first address for one of the memory locations as using a combination of registers for the data cycle when indirect addressing is used thereby using two 8-bit registers for a 16-bit data register (e.g., see col. 4, line 62 to col. 5, line 5);

- (f) if the first data cycle is a write data cycle, transmitting a first datum from the host to the device during a first data cycle, and storing the first datum at the first address in response to detecting the first data cycle as equivalent to a write cycle when the microcontroller is using the 8-bit mode of operation (e.g., see Figure 1); and,
- (g) if the first data cycle is a read data cycle, transmitting a second datum from the device to the host during the first data cycle in response to detecting the first data cycle, the second datum being stored at the first address, wherein the second address cycle is immediately subsequent to the first address cycle, and the first data cycle is immediately subsequent to the second address cycle as equivalent to a read data cycle when the microcontroller is using the 16-bit mode of operation, the first address cycle is immediately followed by the second address cycle and the first data cycle is immediately followed by the second data cycle (e.g., see col. 6, line 63 to col. 7, line 4).

As to claim 2, Wollan teaches the present invention wherein N equals either and M equals 16 (e.g., see col. 4, lines 47-61).

As to claim 3, Wollan teaches the present invention further comprising, if the first and second address portions, when combined, are insufficient to form a first address:

(a) performing a third address cycle to transmit a third address portion over the bus during the third address cycle;

(b) storing the third address portion in a third register of the device in response to detecting the third address cycle;

steps (a) and (b) are taught as the RAM paging feature which adds additional 8-bit external registers to increase the addressing range (e.g., see col. 10, lines 39-5); and,

(e) performing the first data cycle if the first, second, and third address portions, when combined, form a first address for one of the memory locations, wherein the third address cycle is immediately subsequent to the second address cycle, and the first data cycle is immediately subsequent to the third address cycle as each of the 8-bits being combined in a subsequent manner to provide an address space based on 8 bits, 16 bits or as RAM paging using 24 bit addresses and when the address width is established, the data cycle is performed in one cycle for either of the address widths (e.g., see col. 4, line 47 to col. 5, line 39 and col. 10, line 38 to col. 11, line 35).

10. Wollan teaches the invention (claim 12) as claimed including a device comprising:  
at least two requesters, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in a memory space having  $2^M$  addresses, each register associated with a particular count of address-bytes received on a dedicated bus for coupling the device and a processor, the bus having N data lines and at least two control lines, where M is greater than N (e.g., see col. 3, line 59 to col. 4, line 46);  
a memory having a plurality of memory locations (e.g., see Figures 1 and 12);  
a unit to monitor control signals on the bus (e.g., see col. 4, lines 29-46), the unit including:

(a) a K-bit address-byte-received counter to count address-bytes received on the bus by counting each assertion of an address transfer signal on a first control line, wherein the number the number of the registers is less than or equal to  $2^K$  (e.g., see col. 4, lines 29-46);  
(b) selecting unit to selecting unit to select one of the registers according to a count of the address-byte-received counter, wherein the selecting unit selects a distinct one of the registers for a particular count value of the address-byte-received counter (e.g., see col. 4, lines 29-46);

(c) first logic to store an address-byte received on the bus in a currently selected register and to combine address-bytes stored in the registers to form an address for one of the memory locations in response to detecting an assertion of the address transfer signal as logic which determines whether the mode of operation will be 8-bit, 16-bit or 24-bit operational mode (e.g., see col. 4, lines 29-46 and col. 10, lines 28-64); and,

(d) second logic to store a data-byte received on the bus at the address in response to detecting a de-assertion of the address transfer signal and assertion of a write signal, to fetch a data-byte stored at the address from the memory in response to detecting a de-assertion of the address transfer signal and assertion of a read signal, and to reset the address-byte received counter in response to detecting a de-assertion of the address transfer signal and assertion of either a read or write signals as being inherent. The reference does not specifically mention detecting assertion signals or de-assertion signals, however, control operations such as address signals and data transfer operations for 8-bit, 16-bit and 24-bit operations are being performed which indicates such signals are being performed.

As to claim 13, Wollan teaches the present invention wherein N equals eight and M equals N (e.g., see col. 4, lines 47-61).

11. Wollan teaches the invention (claim 23) as claimed including a machine readable medium embodying a program of instructions for execution by a machine to perform a method for accessing a device by a host using a dedicated bus, the device having up to 2M memory locations, the bus having N data lines and at least two control lines, wherein M is greater than N, and the host performs an address cycle by asserting a first control signal and a data cycle by de-asserting the first control signal, comprising:

(a) performing a first address cycle to transmit a first address portion over the bus during the first address cycle;

(b) storing the first address portion in a first register of the device in response to detecting the first address cycle;

steps (a) and (b) are taught as transmitting and storing the first half of a sixteen bit address (e.g., see col. 4, lines 20-28);

(c) performing a second address cycle to transmit a second address portion over the bus during the second address cycle;

(d) storing the second address portion in a second register of the device in response to detecting the second address cycle;

steps (c) and (d) are taught as transmitting and storing the second half of the sixteen bit address (e.g., see col. 4, lines 20-28);

(e) performing a first data cycle if the first and second address portions, when combined, form a first address for one of the memory locations as performing a first data cycle for a 16-bit address operation (e.g., see Table I in col. 12);

(f) if the first data cycle is a write data cycle, transmitting a first datum from the host to the device during the first data cycle, and storing the first datum at the first address in response to detecting the first data cycle (e.g., see Table I in col. 12); and,

(g) if the first data cycle is a read data cycle, transmitting a second datum from the device to the host during the first data cycle in response to detecting the first data cycle, the second datum being stored at the first address, wherein the second address cycle is immediately subsequent to the first address cycle and the first data cycle is immediately subsequent to the second address cycle as equivalent to a read data cycle when the microcontroller is using the 16-

bit mode of operation, the first address cycle is immediately followed by the second address cycle and the first data cycle is immediately followed by the second data cycle (e.g., see col. 6, line 63 to col. 7, line 4).

12. Wollan teaches the invention (claim 23) as claimed including a system comprising:

a central processing unit (e.g., see Figure 1 with support at col. 3, lines 59-65);

a device having:

at least two registers, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in a memory space having  $2^M$  addresses (e.g., see col. 4, lines 47-61);

a memory having a plurality of memory locations (e.g., see Figure 1 with support at col. 3, lines 59-65);

a unit to monitor control signals on the bus as ALU-1 and ALU-2 (e.g., see Figures 1-2), the unit including:

(a) a K-bit address-byte-received counter to count address-bytes received on a bus by counting each assertion of an address transfer signal on a first control line, wherein the number of the registers is less than or equal to  $2^K$  (e.g., see Figure 1 with support at col. 4, lines 6-61);

(b) a selecting unit to select one of the two registers according to a count of the address-byte-received counter, wherein the selecting unit selects a distinct one of the registers for a particular count value of the address-byte-received counter (e.g., see Figure 1 with support at col. 4, lines 6-61);

(c) first logic to store an address-byte received on the bus in a currently selected register and to combine address-bytes stored in at least two registers to form an address

for one of the memory locations in response to detecting an assertion of the address transfer signal as logic which determines whether the mode of operation will be 8-bit, 16-bit or 24-bit operational mode (e.g., see col. 4, lines 29-46 and col. 10, lines 28-64); and,

(d) second logic to store a data-byte received on the bus at the address in response to detecting a de-assertion of the address transfer signal and assertion of a write signal, to fetch a data-byte stored at the address from the memory in response to detecting a de-assertion of the address transfer signal and assertion of a read signal, and to reset the address-byte received counter in response to detecting a de-assertion of the address transfer signal and assertion of either a write or read signals as being inherent. The reference does not specifically mention detecting assertion signals or de-assertion signals, however, control operations such as address signals and data transfer operations for 8-bit, 16-bit and 24-bit operations are being performed which indicate such signals are being performed; and,

the bus to exclusively couple the central processing unit and the device, the bus having N data lines and at least two control lines, where M is greater than N (e.g., see Figure 1).

As to claim 38, Wollan teaches the present invention wherein N equals eight and M equals 16 (e.g., see col. 4, lines 47-61).

### ***RESPONSE TO APPLICANT'S REMARKS***

13. Applicant's arguments filed April 1, 2008 have been fully considered but they are not persuasive.

### ***CONCLUSION***

14. Any inquiry concerning this communication or earlier communications from the

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examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on Monday and Thursday from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2189, Reginald G. Bragdon, can be reached for general questions concerning this application at (571) 272-4204. Additionally, the official fax phone number for the art unit is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

/Reba I. Elmore/  
Primary Patent Examiner  
Art Unit 2189

Saturday, June 14, 2008